

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system comprising:
an application specific integrated circuit (ASIC) ~~adapted for use in a plurality of systems, wherein the system is one of the plurality of systems, and each respective system of the plurality of systems has a circuit configuration that uses a different number of signal channels for further processing by said application specific integrated circuit than do other systems of the plurality of systems comprising a plurality of components for providing a first level of signal channel reduction and a second level of signal channel reduction, wherein said first and second levels of signal channel reduction are achieved by selecting which of said components to enable.~~
2. (Currently Amended) The system of claim 1, wherein said ASIC comprises:
a plurality of multiplexors providing N to M signal multiplexing, wherein in ~~a first configuration of said circuit configurations~~ the first level of signal channel reduction said ASIC is configured to provide N to M signal multiplexing, and wherein in ~~a second configuration of said circuit configuration~~ the second level of signal channel reduction said ASIC is configured to provide N to M/2 signal multiplexing.
3. (Currently Amended) The system of claim 2, wherein said plurality of multiplexors include N signal inputs, M signal outputs, at least one select signal input, and at least one enable signal input, said enable signal input being utilized in providing said N to M/2 signal multiplexing ~~of said second configuration in~~ said second level of signal channel reduction.
4. (Original) The system of claim 3, wherein said plurality of multiplexors are divided into hardwired pairs, and only one of each pair is enabled during a receive operation.
5. (Original) The system of claim 3, wherein at least one of said select signal input and said enable signal input comprise a digital serial control bus.

6. (Currently Amended) The system of claim 1, wherein said ASIC comprises:
a circuit configurable to provide a cross-point switch function in ~~a first configuration of said circuit configurations~~ the first level of signal channel reduction and to provide a signal summer function in the second level of signal channel reduction ~~a second configuration of said circuit configurations~~.

7. (Original) The system of claim 6, wherein said cross-point switch function comprises selectively routing signal channels to one or more beam formers.

8. (Original) The system of claim 6, wherein the signal summer function comprises a symmetric signal summing operation.

9. (Original) The system of claim 8, wherein the symmetric signal summing operation comprises summing one or more signals that are determined to be of similar weight and delay.

10. (Currently Amended) A system comprising:
an application specific integrated circuit (ASIC) ~~adapted for use in a plurality of different circuit configurations, said circuit configurations providing for different numbers of signal channels for further processing using same circuitry of said application specific integrated circuit~~ comprising circuitry enabling selection of a first level of signal channel reduction in a first circuit configuration and enabling selection of a second level of signal channel reduction in a second circuit configuration;

wherein the ASIC is included in an application comprising a transducer, a beam former, and a data path, and wherein the data path is in communication with the ASIC, the transducer, and the beam former.

11. (Original) The system of claim 10, wherein the application further comprises a signal processing unit external to the data path and in communication with the data path at a number of points thereon and is operable to capture and insert information in the data path at each of those number of points.

12. (Currently Amended) A method for using an ASIC that provides a first level of signal channel reduction and a second level of signal channel reduction, the method comprising:
determining a number of signal channels for use in a data path; and
configuring ~~[[an]]the~~ ASIC ~~adapted for use in a plurality of systems, wherein each system has a circuit configuration that uses a different number of channels, to provide said determined number of channels~~ to provide the determined number of signal channels by selecting one or more components in the ASIC to provide the first or second level of signal channel reduction.

13. (Currently Amended) A method of claim 12 further comprising:
~~determining a number of channels for use in a data path;~~
~~configuring an ASIC adapted for use in a plurality of configurations to provide said determined number of channels; and~~
implementing in a sonogram imaging system the ASIC, a first beam former, the data path, and a transducer array, wherein the ASIC, the first beam former, and the transducer array are in communication with the data path.

14. (Original) The method of claim 12 further comprising summing data on each of at least two channels by the ASIC.

15. (Previously Presented) The method of claim 14, wherein summing data comprises:
receiving signals from a control circuit instructing that certain of the channels are to be divided into symmetric pairs and those pairs added, thereby decreasing the number of output channels; and
routing the added pairs to one or more beam formers.

16. (Previously Presented) The method of claim 14, wherein summing data comprises:

receiving signals from a control circuit instructing that certain of the channels are to be divided into adjacent pairs and those pairs added, thereby decreasing the number of output channels; and

routing the added pairs to one or more beam formers.

17. (Original) The method of claim 12 further comprising operating circuitry on the ASIC as a cross-point switch to increase the number of channels from the ASIC to one or more beam formers.

18. (Original) The method of claim 17, wherein operating as a cross-point switch comprises receiving signals from a control circuit instructing that certain of the channels be routed to one or more of the beam formers.

19. (Original) The method of claim 12 further comprising operating circuitry on the ASIC as a plurality of multiplexors, thereby decreasing the number of channels from a transducer array to a beam former.

20. (Original) The method of claim 19, wherein the multiplexors are 2:1 multiplexors, and wherein operating as a plurality of multiplexors comprises selectively enabling one of every two 2:1 multiplexors, thereby providing 4:1 multiplexing functionality.

21. (Original) The method of claim 20, wherein selectively enabling comprises stimulating an enable switch on one of every two 2:1 multiplexors by a control signal from a beam former.

22. (Original) The method of claim 12 further comprising implementing two beam formers in communication with the data path; and

operating the two beam formers and a transducer array to form multiple receive beams.

23. (Original) The method of claim 22 further comprising operating the two beam formers and the transducer array perform a multi-line receive operation.

24. (Previously Presented) The method of claim 12 further comprising implementing a signal processing unit to communicate with the data path at a number of points;

programming the signal processing unit with code to provide a mode of functionality not originally included in a platform using the method; and

operating the signal processing unit to intercept and insert data along the number of points on the path, thereby instructing the platform to perform the mode.

25. (Previously Presented) An apparatus comprising:

a sonogram imaging system including:

a transducer;

a beam former;

a data path including a plurality of information channels connecting the transducer to the beam former; and

an ASIC in communication with the data path between the transducer and the beam former, including circuitry operable as a bank of multiplexors to decrease a number of the information channels from the transducer to the beam former, wherein the circuitry on the ASIC comprises a plurality of 2:1 multiplexors, wherein each mutliplexor includes an enable switch and a select switch, and wherein the beam former controls the enable and select switches on each of the plurality of 2:1 multiplexors to provide a higher-order multiplexing functionality.

26. (Canceled)

27. (Canceled)

28. (Previously Presented) The apparatus of claim 25 further comprising a digital serial control bus to connect the enable and select switches to the beam former.

29. (Currently Amended) An apparatus comprising:
a sonogram imaging system including:
a transducer;
a beam former;
a data path including a plurality of information channels connecting the
transducer to the beam former; and
an ASIC in communication with the data path between the transducer and the
beam former, including circuitry operable as a summer[[/]] and cross-point switch, to route a
number of information channels from the transducer to the beam former;
wherein the circuitry included by the ASIC is controlled by the beam former via a bus
and wherein the beam former sends instructions to logic included in the ASIC via the bus to
process data as a summer.

30. (Original) The apparatus of claim 29, wherein the circuitry included by the ASIC
comprises a summation bus and cross-point switch circuitry.

31. (Previously Presented) The apparatus of claim 30, wherein the summation bus is
operable to decrease a number of information channels between the transducer and the beam
former.

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (New) An apparatus comprising:
a sonogram imaging system including:
a transducer;
a beam former;
a data path including a plurality of information channels connecting the
transducer to the beam former; and
an ASIC in communication with the data path between the transducer and the
beam former, including circuitry operable as a summer and cross-point switch, to route a number
of information channels from the transducer to the beam former;
wherein the circuitry included by the ASIC is controlled by the beam former via a bus
and wherein the beam former sends instructions to logic included in the ASIC via the bus to
process data as a cross-point switch.